This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims

1.-3. (Cancelled)

4. (Amended) The [digital logic device]circuit of claim [1]31, wherein one of [said plurality of generally parallel conductive means]the sets of conductive lines is a plurality of generally parallel doped regions within a semiconductor material.

5. (Amended) The [digital logic device]circuit of claim [4]31, wherein [the other of said plurality of generally parallel conductive means]one of the sets of conductive lines is a plurality of generally parallel metalized regions.

6. (Amended) The [digital logic device]circuit of claim [1]31, wherein said addressing [means]circuitry comprises [means]circuitry to sequentially select [addressed]storage locations.

7. (Amended) The [digital logic device]circuit of claim [1]31, wherein said addressing [means]circuitry comprises [means]circuitry to randomly select [addressed]storage locations.

8. (Amended) The [digital logic device]circuit of claim [1]31, further comprising display means for displaying alphanumeric or graphic information to [its]a user.

9. (Amended) The [digital logic device]circuit of claim [1]31, further comprising input means to enable its user to alter its operation.

10. (Amended) The [digital logic device]circuit of claim [1]31, wherein part or all of said [one more electronic storage means are]circuit is removable or replaceable.

11. (Amended) The [digital logic device]circuit of claim [1]31, wherein output from the [device]circuit is in a digital format.

12. (Amended) The [digital logic device]circuit of claim [1]31, wherein output from the [device]circuit is in an analog format.

13. (Amended) The [digital logic device]circuit of claim [1]31, wherein output from the [device]circuit is in either a digital format or an analog format.

14. – 17. (Cancelled)

18. (Amended) The [storage device]circuit of claim [17]5, wherein said [rectifying conductive means between said plurality of generally parallel doped regions and a plurality of generally parallel metalized regions is]nonlinear elements are of the metal-on-semiconductor junction type.

19. (Amended) The [storage device]circuit of claim [17]5, wherein said [rectifying conductive means between said plurality of generally parallel doped regions and a plurality of generally parallel metalized regions is]nonlinear elements are of the p-n junction type.

20. (Cancelled)

21. (Amended) The [storage device]circuit of claim [14]31, wherein said [rectifying conductive means is comprised by a transistor as the base-emitter junction]nonlinear elements comprise base-emitter junctions of transistors.

22. (Amended) The [storage device]circuit of claim [14]31, further comprising means for retaining the address of the information to be accessed.

23. (Amended) The [storage device]circuit of claim 22, further comprising means for incrementing the retained address.

24. (Amended) The [storage device]circuit of claim 22, further comprising means for setting the retained address.

25. – 27. (Cancelled)

28. (Original) An electronic array of selectable points comprising:

a plurality of conductive means;

a second plurality of conductive means;

a plurality of selectable points where a point of said plurality of selectable points is present in the general vicinity of each point of intersection of each conductive means of the first said plurality of conductive means and each conductive means of the second said plurality of conductive means;

means for selecting a conductive means of one plurality of conductive means, and means for biasing the conductive means of the other plurality of conductive means such that each said selectable point present between a conductive means of said biased plurality of conductive means and a conductive means of the other said plurality of conductive means is potentially forward biased; and

means for selecting a biased conductive means by electronically disabling conductive means within said biased plurality of conductive means by shifting the voltage of those biased conductive means that are to be disabled.

29. (Original) The electronic array of selectable points of claim 28, wherein said means for selecting a conductive means of one plurality of generally parallel conductive means comprises:

means for biasing the conductive means of the said one plurality of conductive means such that each said selectable point present between a conductive means of said biased plurality of conductive means and a conductive means of the other said plurality of conductive means is potentially forward biased; and

means for selecting a biased conductive means by electronically disabling conductive means within said biased plurality of conductive means by shifting the voltage of those biased conductive means that are to be disabled.

30. (Original) The electronic array of selectable points of claim 28, wherein said each selectable point comprises a light emitting diode (LED) which will emit light when forward biased.

31. (New) An information-storage circuit, the circuit comprising:

first and second sets of conductive lines overlapping with each other and defining storage locations at overlap regions;

a pattern of information-defining nonlinear elements, each nonlinear element connected to the first and second sets of conductive lines at an overlap region, presence or absence of a nonlinear element connection at a storage location defining a bit state at the location; and

address circuitry comprising a first pattern of rectifiers directly connected between the first set of conductive lines and a first set of address signal lines, application of an address to the first set of address signal lines causing the first pattern of rectifiers to disable all but one of the first set of conductive lines.

32. (New) The circuit of claim 31 further comprising sensing circuitry for sensing the presence or absence of an information-defining nonlinear element connected to the selected one of the first set of conductive lines and at least a selected one of the second set of conductive lines to thereby determine the bit state at each storage location defined by selected conductive lines.

33. (New) The circuit of claim 31 wherein the all but one of the first set of conductive lines is disabled by shifting a voltage thereon.

34. (New) The circuit of claim 31 further comprising additional address circuitry for disabling all but a selected one of the second set of conductive lines.

35. (New) The circuit of claim 34 wherein the all but one of the second set of conductive lines is disabled by shifting a voltage thereon.

36. (New) The circuit of claim 34 wherein:

the information-defining nonlinear elements have a threshold activation voltage associated therewith;

the address circuitry comprises circuitry for setting all but the selected one of the first set of conductive lines to a first voltage; and

the additional address circuitry comprises circuitry for setting all but the selected one of the second set of conductive lines to a second voltage, the first and second voltages differing by at least the threshold activation voltage.

37. (New) The circuit of claim 36 wherein:

the address circuitry further comprises a first set of selectable disabling lines fewer in number than and connected to the first set of conductive lines by the first pattern of rectifiers, and circuitry for applying a third voltage to at least some of the first set of disabling lines to thereby disable all but one of the first set of conductive lines; and

the additional address circuitry further comprises a second set of selectable disabling lines fewer in number than and connected to the second set of conductive lines by a second pattern of rectifiers, and circuitry for applying a fourth voltage to at least some of the second set of disabling lines to thereby disable all but one of the second set of conductive lines.

38. (New) The circuit of claim 37 wherein the third voltage is substantially equal to the second voltage and the fourth voltage is substantially equal to the first voltage.

39. (New) The circuit of claim 38 wherein all of the rectifiers have said threshold activation voltage associated therewith, application of the threshold activation voltage across the rectifiers allowing current to flow therethrough.

40. (New) The circuit of claim 36 wherein the information-defining nonlinear elements are rectifiers having an associated voltage drop corresponding to the threshold activation voltage, the first and second voltages differing by at least the rectifier voltage drop so that an information-defining rectifier, if connected to the selected conductive lines, is forward biased.

41. (New) The circuit of claim 39 wherein all of the nonlinear elements are rectifiers having an associated voltage drop corresponding to the threshold activation voltage, the first and second voltages differing by at least the rectifier voltage drop.

42. (New) The circuit of claim 36 wherein the second voltage is approximately a ground voltage.

43. (Cancelled)

44. (New) The circuit of claim 32 wherein the sensing circuitry is configured to sense current when said information-defining nonlinear element is not connected to the selected one of the first set of conductive lines and the selected one of the second set of conductive lines.

45. (New) The circuit of claim 44 wherein the sensing circuitry comprises an output line connected to each of the first set of conductive lines by a sensing nonlinear element.

46. (New) The circuit of claim 45 wherein the address circuitry comprises a first set of selectable disabling lines fewer in number than and connected to the first set of conductive lines by the first pattern of rectifiers, and circuitry for applying a second voltage to at least some of the first set of disabling lines to thereby disable all but one of the first set of conductive lines, the information-storage circuit further comprising additional address circuitry which itself comprises (i) a second set of selectable disabling lines fewer in number than and connected to the second set of conductive lines by a second pattern of rectifiers, and (ii) circuitry for applying a first voltage to at least some of the second set of disabling lines to thereby disable all but one of the second set of conductive lines, all of the rectifiers having a threshold activation voltage associated therewith, application of the threshold activation voltage across the rectifiers allowing current to flow therethrough.

47. – 50. (Cancelled)

51. (New) The circuit of claim 31 further comprising a first series of voltage-drop elements connecting the first set of conductive lines to a circuitry for applying a first voltage and a second series of voltage drop elements connecting the second set of conductive lines to a circuitry for applying a second voltage.

52. (New) The circuit of claim 51 wherein the first and second series of voltage drop elements are resistors.

53. (New) The circuit of claim 51 wherein the first and second series of voltage drop elements are nonlinear elements.

54. (New) The circuit of claim 53 wherein the nonlinear elements are rectifiers.

55. (New) The circuit of claim 54, wherein the first and second sets of conductive lines are disposed on an integrated circuit chip, and the circuitry for applying the first voltage and the circuitry for applying the second voltage are disposed off of the integrated circuit chip and connected thereto.

56. (New) The circuit of claim 51 wherein the second voltage is approximately a ground voltage.

57. (New) The circuit of claim 32 further comprising a first series of voltage-drop elements connecting the first set of conductive lines to a circuitry for applying a first voltage and a second series of voltage drop elements connecting the second set of conductive lines to a circuitry for applying a second voltage.

58. (New) The circuit of claim 57 wherein the first and second series of voltage drop elements are resistors.

59. (New) The circuit of claim 57 wherein the first and second series of voltage drop elements are nonlinear elements.

60. (New) The circuit of claim 59 wherein the nonlinear elements are rectifiers.

61. (New) The circuit of claim 60, wherein the first and second sets of conductive lines are disposed on an integrated circuit chip, and the circuitry for applying the first voltage and the circuitry for applying the second voltage are disposed off of the integrated circuit chip and connected thereto.

62. (New) The circuit of claim 57 wherein the second voltage is approximately a ground voltage.

63. (New) The circuit of claim 46 further comprising a first series of voltage-drop elements connecting the first set of conductive lines to a circuitry for applying a first voltage and a second series of voltage drop elements connecting the second set of conductive lines to a circuitry for applying a second voltage.

64. (New) The circuit of claim 63 wherein the first and second series of voltage drop elements are resistors.

65. (New) The circuit of claim 63 wherein the first and second series of voltage drop elements are nonlinear elements.

66. (New) The circuit of claim 65 wherein the nonlinear elements are rectifiers.

67. (New) The circuit of claim 66, wherein the first and second sets of conductive lines are disposed on an integrated circuit chip, and the circuitry for applying the first voltage and the circuitry for applying the second voltage are disposed off of the integrated circuit chip and connected thereto.

68. (New) The circuit of claim 63 wherein the second voltage is approximately a ground voltage.

69. (New) The circuit of claim 31 wherein the circuit operates as a random access memory.

70. (New) The circuit of claim 31 wherein the circuit operates as a read only memory.

71. (New) The circuit of claim 31 wherein the circuit operates as a one-time-programmable read only memory.

72. – 87. (Cancelled)